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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/091,393 | 03/07/2002 | Yossi Rindner | RINDNER=1 | 8666 |

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| EXAMINER | |
|---|---|
| TRUONG, CAM Y T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2162 | |

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/091,393 | RINDNER, YOSSI | |
| | Examiner | Art Unit | |
| | Cam Y T Truong | 2162 | |

*-- Th MAILING DATE of this communication appears on the cover sheet with the correspondenc address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *5-13* is/are pending in the application.

4a) Of the above claim(s) *1-4,14 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's election with traverse of invention II, claims 5-13 in the reply filed on 9/30/2004 is acknowledged. The traversal is on the ground(s) that "claim 1 relates to a method for interfacing between first and second successive stages of an ASIC synthesis tool while claim 5 relates to apparatus for interfacing between first and second successive stages of an ASIC synthesis tool. The script files automatically generated in accordance with claim 1 are the script files relating to each of the selectors of claim 5"

This is not found persuasive because claims 1 and 14-15 are drawn to automatically generating script files, which is used to processing output data in accordance with information contained in the script files, is classified in class 703, subclass 23. In contract, claims 5-13 are drawn to a plurality of selectors corresponding to a tool for performing a stage in an ASIC that is used to access memory and executing command files, is classified in claims 716, subclass 18.

Thus, it is respectfully submitted that the search and examination of the entire application would be made with serious burden.

The requirement is still deemed proper and is therefore made FINAL.

Claims 1-4, and 14-15 are not selected; thus they are withdrawn from consideration.

Claims 5-13 are pending in this Office Action.

### *Claim Objections*

2. Claims 5, 9 and 12 are objected to because of the following informalities:

The reference characters "ASIC" in claim 5 on page 3, lines 5-10 should be spelled out.

Claim 9 recites the claimed limitation "wherein the pre-prepared template is part of the selected selectors" on page 4, lines 6-7. The language for this claimed limitation is incorrect according to the description of the application, a template includes a plurality of selectors i.e. button (fig. 1, page 7, lines 15-18). Thus, base on the description of the application, examiner interprets this claimed limitation as the selected selectors are parts on the pre-prepared template.

Claim 12 recites the claimed limitation "wherein the commands executed by the processor are parts of each of said selected selectors". The language for this claimed limitation is incorrect according to the description of the application, command files, i.e. scripts, relating to each selectors (page 7, line 21); thus, examiner interprets this claimed limitation as the commands executed by the processor are related to each of said selected selectors.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 5, 6, 9, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Duboc et al (or hereinafter "Duboc") (US 6425116).

As to claim 5, Duboc teaches an apparatus for interfacing between first and second successive stages of an ASIC synthesis tool (fig. 5, col. 8, lines 25-36), said apparatus comprising:

"a processor" as processor 31 (fig. 2),

"a plurality of selectors coupled to the processor" as a compile button 224 and a cancel option is provided by a close button 226, optional circuit blocks that can select by a user via a user interface are coupled to the processor 31. The buttons and circuit blocks are represented as selectors (figs. 2&6, col. 10, lines 20-25; col. 5, lines 60-63);

"each corresponding to a tool for performing a stage in an ASIC design" as a compile option or button 224 is corresponding to the HDL Integrator tool. Circuit blocks are corresponding to a design reuse tool or the HDL Integrator tool. The user initiates generation of the integrated circuit design via selection of a compile option or button 224 from the GUI window. In this case, the step user initiates generation of the integrated circuit design via selection of a compile option from the GUI window is represented as a stage in a circuit design (col. 8, lines 33-38; col. 10, lines 20-25; col. 5, lines 60-63);

"a memory coupled to the processor and storing therein respective script files relating to each of said selectors" as memory 32 is coupled to processor 31. The template may also generate one or more script files, including IIDLI scripts utilized to extract instantiated blocks from the design reuse tool database to extract instantiated

blocks from the design reuse tool database. In addition, scripts for running the memory Integrator tool, as well as compilation and simulation script, may be generated to simulate the subsystem. The above information implies that generated script files has stored in the memory for extracting instantiated blocks as selectors (fig. 5, col. 10, lines 58-64);

"said processor being responsive to selection of at least one of the selectors for accessing the memory and executing commands associated therewith" as processor 31 being responsive to selection of a compile option from the GUI window for accessing the memory and executing a check script 154 and a build script 162. Script 153 and 162 are represented as commands associated with the compile option (figs. 2&5, col. 8, lines 33-49).

As to claim 6, Duboc teaches the claimed limitation "wherein the commands executed by the processor are extracted from the respective script file relating to each of said selected selectors" as processor 31 being responsive to selection of a compile option from the GUI window for accessing the memory to retrieve instructions of the check script 154 from a script file related to selected blocks or compile option (figs. 2&5, col. 8, lines 33-49; col. 10, lines 58-60).

As to claim 9, Duboc teaches the claimed limitation "wherein the pre-prepared template is part of the selected selector" as indicated on the above claims objection, this

claimed language is considered as the selected selector such as button 224 is part of template as DSP builder template (fig. 6).

As to claim 12, Duboc teaches the claimed limitation "wherein the commands executed by the processor are parts of each of said selected selectors" as indicated on the above claims objection, this claimed language is considered as the commands executed by the processor are related the each of said selected selector. Build script 162 and script 154 are related to compile or button 224 and close or button 226 (fig. 6, col. 8, lines 33-50).

As to claim 13, Duboc teaches the claimed limitation "wherein at least some of said selectors are operable via a graphic user interface" as template permits both the selection of one or more optional circuit blocks and the customization of one or more customizable circuit blocks to be performed via a user interface (col. 5, lines 60-63).

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Gupte et al (or hereinafter "Gupte") (US 5903475).

As to claim 7, Duboc discloses the claimed limitation subject matter in claim 6, except the claimed limitation "wherein the script file relating to each of said selected selectors is automatically generated". Gupte teaches automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs (col.13, lines 25-35).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

As to claim 8, Duboc discloses the claimed limitation subject matter in claim 6, except the claimed limitation "wherein the script file relating to each of said selected selectors is automatically generated according to a pre-prepared template". Duboc teaches a template may also generate one or more script files (col. 10, lines 58-60). Gupte teaches automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs (col.13, lines 25-35).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

7. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Gupte and further in view of Hekmatpour (US 2002/0156929).

As to claim 10, Duboc and Gupte disclose the claimed limitation subject matter in claim 8, except the claimed limitation "wherein the pre-prepared template is a pre-prepared external file". Hekmatpour teaches XML file, which is represented as an external file (fig. 4, page 3, col. Left, line 41).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Hekmatpour's teaching of XML file to Duboc's system and Gupte's system in order to provide a system for enabling collaborative design and verification of a system on a chip (Soc) and further to generate a plurality of functional components that includes simulator and synthesis and timing analysis component.

As to claim 11, Duboc and Gupte disclose the claimed limitation subject matter in claim 8, except the claimed limitation "wherein the pre-prepared external template file is

an XML file". Hekmatpour teaches XML file, which is represented as an external file (fig. 4, page 3, col. Left, line 41).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Hekmatpour's teaching of XML file to Duboc's system and Gupte's system in order to provide a system for enabling collaborative design and verification of a system on a chip (Soc) and further to generate a plurality of functional components that includes simulator and synthesis and timing analysis component.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dockser et al (US 5963454) disclose creating HDL template (abstract). This subject matter is relevance for claim 5.

**C ntact Information**

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cam Y T Truong whose telephone number is (571) 272-4042. The examiner can normally be reached on Monday to Firday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cam-Y Truong
Patent Examiner
Art Unit 2162
1/3/2005